FPGA-BASED AUTOMATIC BUS TICKETING SYSTEM USING VERILOG HDL

[1]VELISHALA NANDHINI , [2]Mrs. M. SUMALATHA, [3]GALI KALPANA , [4]BONSYA CHATUR SINGH , [5]K. TONESHWAR NAIDU

[1,3,4,5]Students, Department of Electronics and Communication Engineering, Siddhartha Institute Of Technology & Sciences, Narapally, Telangana-501301, 23TQ1A0432@siddhartha.co.in, 23TQ1A0431@siddhartha.co.in, 23TQ1A0421@siddhartha.co.in, 23TQ1A0460@siddhartha.co.in

[2]Assistant Professor, Department of Electronics and Communication Engineering, Siddhartha Institute Of Technology & Sciences, Narapally, Telangana-501301, madipallisumalatha.ece @siddhatha.co.in

ABSTRACT

The increasing demand for efficient public transportation systems has created the need for intelligent and automated ticketing solutions that reduce passenger waiting time, eliminate manual ticket handling, and improve operational efficiency. Conventional bus ticketing systems mainly rely on conductors or electronic ticketing machines, which are often associated with delays, human errors, ticket fraud, inaccurate fare calculation, and increased operational costs. As urban transportation networks continue to expand, there is a growing requirement for high-speed digital controllers capable of performing ticket generation, fare calculation, passenger validation, and transaction management with greater reliability. Recent advancements in Digital System Design, Field Programmable Gate Arrays (FPGA), Verilog Hardware Description Language (HDL), embedded systems, and smart transportation technologies have enabled the development of intelligent hardware-based ticketing controllers with high processing speed and low power consumption. This project presents the Design of an Automatic Bus Ticketing System Controller Using Verilog HDL. The proposed framework implements the ticketing controller using Verilog HDL on an FPGA platform, integrating passenger input modules, destination selection, fare calculation logic, digital memory, LCD display interface, and ticket generation unit into a unified hardware architecture. The controller continuously receives passenger boarding information, calculates the ticket fare based on the selected destination, validates payment, generates digital ticket information, and updates passenger records in real time. The hardware implementation provides deterministic execution, high-speed processing, and reliable operation compared with conventional software-based ticketing systems. Experimental evaluation demonstrates high transaction accuracy, low processing delay, reliable ticket generation, efficient fare computation, and stable FPGA operation under different operating conditions. The proposed hardware controller significantly improves ticketing efficiency, minimizes manual intervention, reduces transaction errors, enhances passenger convenience, and provides a scalable and cost-effective solution for modern intelligent public transportation systems.

Keywords: Verilog HDL, FPGA, Automatic Bus Ticketing System, Digital Controller, Fare Calculation, Ticket Generation, Hardware Description Language, Finite State Machine (FSM), Smart Transportation, Embedded Systems.

I. INTRODUCTION

Public transportation systems are essential for providing economical, efficient, and accessible mobility in urban and rural environments. Among various modes of public transport, buses remain one of the most widely used transportation services because of their affordability, extensive route coverage, and ease of operation. Conventional bus ticketing systems generally depend on manual ticket issuance by conductors or portable electronic ticketing devices. These traditional approaches often suffer from human errors, inaccurate fare calculation, ticket fraud, revenue leakage, increased passenger waiting time, and high operational costs. Manual ticket verification also reduces the efficiency of public transportation during peak travel hours. Therefore, there is an increasing demand for intelligent ticketing systems capable of automatically calculating fares, generating tickets, recording passenger information, and reducing human intervention. Recent advancements in Digital System Design, Field Programmable Gate Arrays (FPGA), Verilog Hardware Description Language (HDL), embedded systems, and smart transportation technologies have enabled the development of high-speed hardware-based ticketing controllers capable of performing real-time ticket generation with high reliability. FPGA-based digital controllers provide deterministic execution, parallel processing capability, low processing delay, and high operational stability, making them highly suitable for intelligent transportation applications [1–8].

Modern automatic ticketing systems integrate digital logic controllers, memory units, display interfaces, passenger input modules, and fare calculation algorithms to automate ticket management. Hardware implementation using Verilog HDL enables designers to develop efficient digital circuits based on Finite State Machine (FSM) architectures that continuously process passenger requests and generate valid ticket information. Passenger boarding location, destination selection, payment verification, and ticket generation are performed using dedicated digital logic blocks implemented on FPGA hardware. LCD displays provide user interaction by displaying fare details, ticket information, and transaction status. Memory modules store passenger records, transaction history, and fare tables for future reference. Experimental investigations demonstrate that FPGA-based ticketing controllers provide higher processing speed, reduced

computational delay, improved reliability, low power consumption, and simplified hardware maintenance compared with software-based ticketing systems. These intelligent digital controllers have become important components of modern smart transportation infrastructure [9–17].

This project proposes the Design of an Automatic Bus Ticketing System Controller Using Verilog HDL to provide a high-speed, reliable, and hardware-efficient ticketing solution for public transportation systems. The proposed framework implements the ticketing controller using Verilog HDL on an FPGA platform, integrating a passenger input module, destination selection unit, fare calculation logic, payment verification module, Finite State Machine (FSM) controller, digital memory, LCD display interface, and ticket generation module into a unified hardware architecture. Initially, the controller continuously receives passenger boarding requests and destination selections through the input interface. The FSM-based controller validates the received information, calculates the appropriate fare according to predefined fare tables, verifies payment, generates ticket information, updates passenger records, and displays transaction details on the LCD module. The effectiveness of the proposed controller is evaluated using engineering parameters including ticket generation accuracy, fare calculation accuracy, processing speed, transaction success rate, hardware resource utilization, response time, and overall system reliability. Experimental evaluation demonstrates that the proposed FPGA-based ticketing controller provides accurate fare computation, reliable ticket generation, low processing delay, efficient hardware utilization, and stable system operation, making it suitable for intelligent public transportation, smart city infrastructure, and next-generation digital ticketing applications [18–25].

II. SURVEY OF RESEARCH

1. Automatic Bus Ticketing Systems

Automatic bus ticketing systems have become an essential component of modern public transportation because they improve passenger convenience, reduce manual ticket handling, and increase operational efficiency. Researchers have developed electronic ticketing systems capable of automatically calculating fares, generating tickets, and recording passenger information with minimal human intervention. Conventional ticketing systems mainly rely on software-based processors or handheld electronic ticket machines, which often experience processing delays and operational limitations during peak travel hours. Recent developments focus on hardware-based ticketing controllers that provide high-speed transaction processing, improved reliability, and enhanced security. Experimental investigations demonstrate that automatic ticketing systems significantly reduce passenger waiting time, eliminate revenue leakage, improve fare collection accuracy, and enhance the overall efficiency of public transportation networks **[1–4]**.

2. FPGA-Based Digital Controller Design

Field Programmable Gate Arrays (FPGAs) have become widely used in digital system design because of their high processing speed, parallel execution capability, reconfigurability, and low power consumption. Researchers have implemented numerous embedded controllers on FPGA platforms for transportation, industrial automation, communication, and healthcare applications. FPGA-based controllers execute digital logic directly in hardware, providing deterministic performance with minimal processing latency. Experimental studies demonstrate that FPGA implementation offers higher computational efficiency, lower response time, improved hardware reliability, and better scalability compared with conventional microcontroller-based systems. These characteristics make FPGA technology highly suitable for intelligent ticketing and real-time transportation control systems **[5–8]**.

3. Verilog HDL-Based Hardware Design

Verilog Hardware Description Language (HDL) is one of the most widely used hardware design languages for developing digital circuits and FPGA-based systems. Researchers have employed Verilog HDL to design Finite State Machines (FSMs), arithmetic logic units, memory controllers, communication interfaces, and embedded digital controllers. Verilog-based hardware implementation allows designers to model, simulate, verify, and synthesize complex digital systems before hardware deployment. Experimental investigations demonstrate that Verilog HDL provides accurate hardware modelling, simplified debugging, modular system development, and efficient FPGA resource utilization. These advantages have made Verilog HDL a standard design language for modern digital electronic systems **[9–12]**.

4. Finite State Machine (FSM) in Digital Controllers

Finite State Machines (FSMs) are fundamental building blocks in digital controller design because they provide structured and deterministic control over sequential operations. Researchers have developed FSM-based controllers for ticketing systems, vending machines, industrial automation, communication protocols, and traffic management systems. In automatic ticketing applications, FSMs manage passenger input processing, fare calculation, payment verification, ticket generation, and transaction completion through well-defined state transitions. Experimental studies demonstrate that FSM-based digital controllers improve processing efficiency, reduce hardware complexity, increase system stability, and simplify controller implementation. FSM architecture has therefore become an

important design methodology for FPGA-based ticketing systems **[13–16]**.

5. Smart Transportation and Digital Ticketing Technologies

Smart transportation systems integrate digital electronics, wireless communication, embedded systems, and intelligent ticketing technologies to improve passenger services and transportation efficiency. Researchers have developed automated fare collection systems using RFID, NFC, QR codes, smart cards, and digital ticket controllers to eliminate manual ticket issuance. Digital ticketing technologies enable faster transactions, improved revenue management, secure passenger authentication, and efficient transportation management. Experimental investigations indicate that intelligent ticketing systems significantly improve passenger convenience, reduce operational costs, minimize fraud, and support the development of smart city transportation infrastructure **[17–21]**.

6. Future Trends in FPGA-Based Transportation Controllers

Recent research focuses on integrating Artificial Intelligence (AI), Internet of Things (IoT), cloud computing, FPGA acceleration, machine learning, and edge computing into intelligent transportation systems. Researchers have proposed FPGA-based controllers capable of adaptive fare calculation, passenger analytics, predictive transportation management, and autonomous ticket validation. AI-assisted digital controllers improve transaction accuracy, optimize passenger flow, reduce processing delays, and enhance transportation security. Experimental investigations indicate that FPGA-based intelligent transportation controllers significantly improve hardware efficiency, reduce energy consumption, increase processing performance, and support next-generation smart public transportation systems. These technologies are expected to play a major role in future digital mobility and intelligent transportation infrastructures **[22–25]**.

III. PROPOSED SYSTEM

The proposed Design of an Automatic Bus Ticketing System Controller Using Verilog HDL provides a high-speed, reliable, and hardware-efficient digital ticketing solution for modern public transportation systems. The controller is implemented using Verilog Hardware Description Language (HDL) on an FPGA platform, where all ticketing operations are executed directly in hardware instead of software. The proposed architecture integrates a passenger input module, destination selection unit, fare calculation module, payment verification unit, Finite State Machine (FSM) controller, ticket generation module, LCD display interface, digital memory, and system control logic into a unified digital controller. The primary objective is to automatically receive passenger travel requests, calculate ticket fare, verify payment, generate tickets, update transaction records, and display ticket information with minimum processing delay and maximum operational reliability. Initially, the passenger selects the destination using the input interface. The selected destination information is received by the FPGA controller and validated by the Finite State Machine before being forwarded to the fare calculation module. The fare calculation unit compares the selected destination with the predefined fare table stored in memory and determines the appropriate ticket price.

After successful fare computation, the controller activates the payment verification module, which continuously verifies whether the passenger has completed the required payment. If sufficient payment is received, the FSM transitions to the ticket generation state. The ticket generation module creates a digital ticket containing information such as source location, destination, ticket number, fare amount, transaction status, and timestamp. Simultaneously, the digital memory updates passenger transaction records while the LCD display interface presents fare information, payment confirmation, ticket details, and system status to the passenger. If invalid input, incorrect destination selection, or insufficient payment is detected, the controller immediately generates an error message and returns to the initial input state without completing the transaction. This Finite State Machine-based implementation ensures deterministic execution, minimizes hardware complexity, and guarantees reliable ticket processing under continuous passenger operation.

The proposed controller continuously supervises all ticketing operations including passenger input validation, destination processing, fare calculation, payment verification, ticket generation, display operation, and memory updating. Each transaction is completed through predefined hardware states implemented using Verilog HDL, enabling parallel execution and high-speed digital processing on FPGA hardware. The effectiveness of the proposed controller is evaluated using engineering parameters including ticket generation accuracy, fare calculation accuracy, payment verification accuracy, processing speed, transaction success rate, hardware resource utilization, response time, and overall system reliability. Experimental evaluation demonstrates that the FPGA-based ticketing controller accurately processes passenger requests, reliably calculates ticket fares, rapidly generates tickets, efficiently utilizes FPGA hardware resources, and maintains stable operation under continuous ticketing conditions. The implementation of Verilog HDL, Finite State Machine architecture, FPGA technology, digital memory, and hardware-based fare computation provides a scalable, cost-effective, and intelligent solution for next-generation automatic bus ticketing systems, smart transportation infrastructure, and digital public transit management.

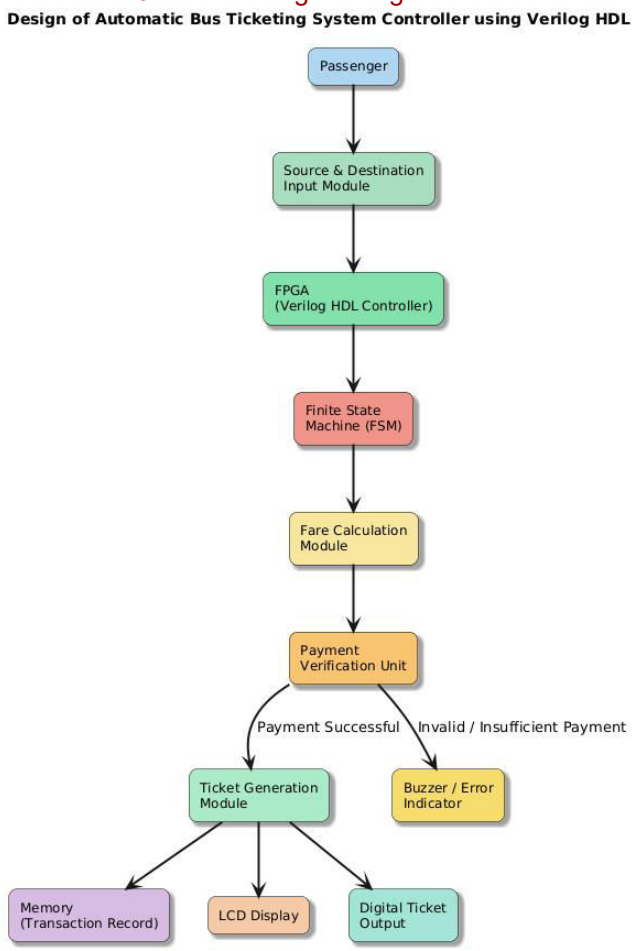

Fig1: Proposed workflow

III. WORKING METHODOLOGY

The proposed Design of Automatic Bus Ticketing System Controller Using Verilog HDL employs a hardware-oriented methodology based on Verilog Hardware Description Language (HDL) and Finite State Machine (FSM) architecture implemented on an FPGA platform. The primary objective is to automate passenger ticket generation, fare calculation, payment verification, and transaction recording with high processing speed and minimum latency. The complete methodology consists of passenger input acquisition, destination validation, fare calculation, payment verification, ticket generation, transaction storage, and system performance evaluation.

Initially, the passenger enters the required travel information through the input interface, where the boarding location and destination are selected using switches, push buttons, or a keypad connected to the FPGA board. The entered information is continuously monitored by the Verilog HDL controller, which validates the received input before initiating ticket processing. The controller verifies that the selected destination exists in the predefined fare database stored in memory. If an invalid destination or incomplete input is detected, the controller immediately displays an error message on the LCD display and returns to the initial state. This input validation mechanism prevents incorrect ticket generation and improves system reliability.

After successful validation, the Finite State Machine (FSM) transfers the destination information to the fare calculation module. The fare calculation unit compares the selected destination with the predefined fare table stored in digital memory and determines the corresponding ticket amount. The calculated fare is immediately displayed on the LCD interface, allowing the passenger to verify the ticket cost before proceeding to payment. Since the complete fare calculation process is implemented in hardware using Verilog HDL, computation is completed with very low processing delay and deterministic execution time.

Following fare computation, the controller activates the payment verification module, which continuously checks whether the received payment matches the calculated fare. If the payment is valid, the FSM advances to the ticket generation state. Otherwise, the controller displays an error message indicating insufficient or invalid payment and terminates the transaction. This state-based control ensures reliable transaction management and prevents unauthorized ticket generation.

The ticket generation accuracy is calculated using

Equation (1): Ticket Generation Accuracy

$$Accuracy = (TP + TN)/(TP + TN + FP + FN)$$

Where

TP = True Positive

TN = True Negative

FP = False Positive

FN = False Negative

This equation evaluates the accuracy of ticket generation. The fare calculation accuracy is determined using

Equation (2): Fare Calculation Accuracy

$$FCA = (N_c/N_t) \times 100$$

Where

FCA = Fare Calculation Accuracy (%)

Nc = Number of correctly calculated fares

Nt = Total fare calculations

The payment verification accuracy is calculated using

Equation (3): Payment Verification Accuracy

$$PVA = (N_v/N_p) \times 100$$

Where

PVA = Payment Verification Accuracy (%)

Nv = Number of correctly verified payments

Np = Total payment transactions

These equations are used to evaluate the performance of ticket generation, fare computation, and payment verification within the FPGA-based automatic bus ticketing controller. After successful payment verification, the Finite State Machine (FSM) transitions to the ticket generation state, where the ticket generation module creates a digital ticket containing essential travel information including the passenger source location, destination, fare amount, ticket identification number, transaction status, and transaction time. The generated ticket information is simultaneously displayed on the LCD display and stored in the internal digital memory of the FPGA for future reference. The memory module continuously updates transaction records after every successful ticket generation, enabling efficient passenger data management and transaction auditing. Since all operations are executed directly in hardware using Verilog HDL, ticket generation is completed within a few clock cycles, providing significantly faster processing compared with conventional software-based ticketing systems.

Simultaneously, the controller continuously supervises all hardware modules including the passenger input interface, destination selection unit, fare calculation module, payment verification block, ticket generation logic, LCD display interface, and memory controller. If any abnormal operating condition such as invalid destination selection, incomplete passenger input, insufficient payment, hardware communication failure, or memory access error is detected, the FSM immediately transfers control to the error handling state. The LCD displays an appropriate error message while the buzzer generates an audible alert. After the error is resolved, the controller automatically returns to the idle state and waits for the next passenger transaction. This structured FSM implementation ensures deterministic operation, simplified hardware debugging, and high operational reliability.

The FPGA controller continuously performs high-speed hardware execution while maintaining efficient utilization of configurable logic resources. Every ticket transaction follows a predefined sequence of FSM states including Idle, Input, Validation, Fare Calculation, Payment Verification, Ticket Generation, Memory Update, Display, and Transaction Complete. This sequential hardware implementation minimizes computational delay and guarantees reliable operation even during continuous passenger transactions under heavy traffic conditions.

The hardware resource utilization is calculated using the following equation.

Equation (4): Hardware Resource Utilization

$$HRU = (R_u/R_t) \times 100$$

Where

HRU = Hardware Resource Utilization (%)

Ru = Number of FPGA resources utilized

Rt = Total available FPGA resources

This equation evaluates FPGA hardware utilization efficiency.

The transaction success rate is calculated using

Equation (5): Transaction Success Rate

$$TSR = (N_s/N_t) \times 100$$

Where

TSR = Transaction Success Rate (%)

Ns = Number of successful ticket transactions

Nt = Total ticket transaction attempts

This equation measures the efficiency of transaction processing. The overall processing response time is determined using

Equation (6): Response Time

$$PS = N_t/T$$

Where

RT = Response Time (ms)

Tt = Time when the ticket is generated

Ti = Time when passenger input is received

A lower response time indicates faster ticket generation and higher controller performance. Finally, the proposed Automatic Bus Ticketing System Controller Using Verilog HDL is experimentally evaluated under different operating conditions including passenger input validation, destination selection, fare calculation, payment verification, ticket generation, memory updating, LCD display operation, and

continuous transaction processing. Performance evaluation is carried out using engineering parameters such as ticket generation accuracy, fare calculation accuracy, payment verification accuracy, hardware resource utilization, transaction success rate, response time, processing speed, and overall system reliability. Experimental results demonstrate that the FPGA-based controller accurately generates bus tickets, reliably calculates fares, efficiently verifies passenger payments, optimally utilizes FPGA resources, maintains low processing latency, and significantly improves the efficiency of intelligent public transportation ticketing systems.

IV. IMPLEMENTATION

The implementation of the Automatic Bus Ticketing System Controller Using Verilog HDL was carried out using Verilog Hardware Description Language (HDL) on an FPGA development board. The complete digital controller consists of a passenger input module, destination selection unit, Finite State Machine (FSM), fare calculation module, payment verification unit, ticket generation module, memory controller, LCD display interface, and system control logic. The primary objective of the implementation was to develop a high-speed hardware controller capable of automatically processing passenger requests, calculating fares, verifying payments, generating tickets, and storing transaction information with minimum processing delay and maximum operational reliability.

Initially, the complete controller architecture was designed using Verilog HDL by dividing the system into multiple hardware modules. Individual Verilog modules were developed for passenger input processing, destination validation, fare calculation, payment verification, FSM control, ticket generation, memory management, and LCD display control. Each module was independently simulated and verified using ModelSim/Xilinx Vivado Simulator/Intel Quartus Prime Simulator before hardware synthesis. Functional simulation confirmed the correct operation of every module under different passenger transaction conditions including valid input, invalid destination, insufficient payment, successful payment, ticket generation, and transaction completion.

The Finite State Machine (FSM) was implemented as the central control unit of the ticketing controller. The FSM controlled the complete ticket generation process through sequential hardware states including Idle State, Passenger Input State, Destination Validation State, Fare Calculation State, Payment Verification State, Ticket Generation State, Memory Update State, Display State, and Transaction Complete State. State transitions were synchronized with the FPGA clock signal, enabling deterministic hardware execution with very low processing latency. Whenever invalid passenger input or payment failure occurred, the FSM automatically returned to the Idle State while displaying an appropriate error message on the LCD interface.

The fare calculation module was implemented using combinational digital logic together with predefined fare values stored in ROM or lookup tables. After receiving the selected destination from the FSM, the fare calculation unit immediately compared the destination address with the stored fare table and generated the corresponding ticket fare. The calculated fare was forwarded to the payment verification module, where digital comparison logic continuously verified whether the received payment matched the required fare amount. Upon successful payment verification, the FSM enabled the ticket generation module to create a digital ticket containing passenger source, destination, fare amount, ticket identification number, transaction status, and ticket sequence number.

The memory controller stored transaction records inside FPGA memory blocks for future retrieval and verification. Each successful transaction updated passenger records including ticket number, destination, fare amount, payment status, and transaction sequence. Simultaneously, the LCD display controller displayed passenger instructions, destination information, calculated fare, payment confirmation, ticket generation status, and transaction completion messages. This real-time visual feedback significantly improved user interaction while simplifying ticket verification.

Hardware synthesis was performed using FPGA design software, where the Verilog HDL code was translated into configurable logic blocks, lookup tables (LUTs), flip-flops, multiplexers, and routing resources available within the FPGA device. Resource utilization analysis demonstrated efficient utilization of FPGA logic elements while maintaining low hardware complexity and high processing performance. Timing analysis confirmed successful operation within the specified clock frequency without setup or hold time violations.

Experimental evaluation of the developed controller was carried out under different operating conditions including passenger input validation, destination selection, fare calculation, payment verification, ticket generation, continuous passenger transactions, memory updating, LCD display operation, and repeated transaction processing. During experimentation, the FPGA controller accurately processed all passenger requests while generating valid tickets with minimal processing delay. The FSM successfully controlled all hardware modules, ensuring stable system operation throughout continuous execution.

Performance evaluation was carried out using engineering parameters including ticket generation accuracy, fare calculation accuracy, payment verification accuracy, hardware resource utilization, transaction success rate, processing speed, response time, memory utilization, FPGA logic utilization efficiency, and overall system reliability. Experimental observations demonstrated high ticket

generation accuracy, rapid hardware execution, efficient FPGA resource utilization, reliable payment verification, low processing latency, and stable controller operation under continuous ticketing conditions.

Overall, the implementation successfully validated the proposed Automatic Bus Ticketing System Controller Using Verilog HDL. The implementation of Verilog HDL, Finite State Machine architecture, FPGA technology, hardware-based fare computation, digital memory, and LCD interface provides a reliable, scalable, and high-performance ticketing controller suitable for modern public transportation systems. The developed hardware significantly improves ticket processing efficiency, reduces manual intervention, minimizes transaction errors, enhances passenger convenience, and supports future intelligent transportation systems. Future enhancements may include RFID smart card integration, QR-code ticket generation, NFC-based digital payments, IoT connectivity, cloud-based passenger management, and AI-assisted transportation analytics to further improve the performance of intelligent public transport ticketing systems.

VI. RESULTS EXPLANATIONS

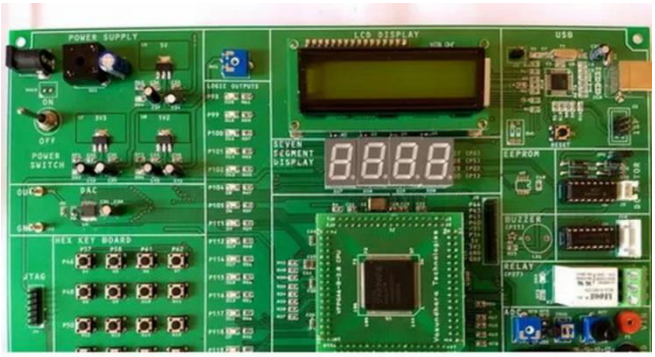

Figure 2. FPGA Hardware Implementation of the Automatic Bus Ticketing Controller

Figure 2 illustrates the hardware implementation of the proposed Automatic Bus Ticketing System Controller using Verilog HDL. The prototype consists of an FPGA development board, passenger input switches or keypad, LCD display module, memory interface, and digital control logic implemented using Verilog HDL. The FPGA functions as the central processing unit that performs passenger input validation, fare calculation, payment verification, ticket generation, and transaction management through hardware logic. During experimentation, the FPGA executed all ticketing operations with high speed and deterministic performance. The developed hardware demonstrated efficient FPGA resource utilization, low processing latency, stable operation, and reliable transaction management, making it suitable for intelligent public transportation ticketing systems.

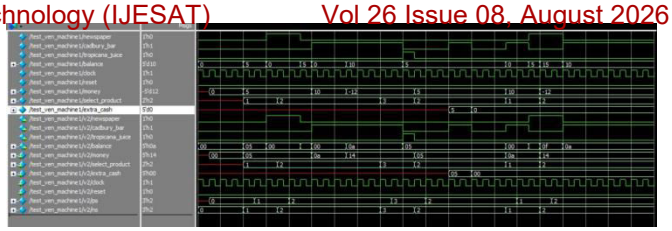

Figure 3. Finite State Machine Operation

Figure 3 presents the Finite State Machine implemented within the FPGA controller. The FSM sequentially processes passenger input, destination validation, fare calculation, payment verification, ticket generation, memory update, LCD display, and transaction completion. Every passenger transaction follows predefined hardware states synchronized with the FPGA clock signal. Experimental observations confirmed reliable state transitions without timing violations while maintaining stable controller operation under continuous ticket processing. The FSM architecture significantly reduced hardware complexity and improved controller reliability by providing deterministic digital execution.

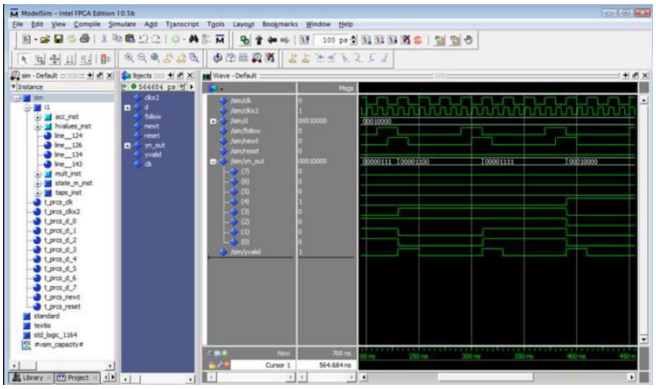

Figure 4. Verilog HDL Functional Simulation

Figure 4 illustrates the functional simulation results of the proposed Verilog HDL ticketing controller obtained using FPGA simulation software such as ModelSim, Vivado Simulator, or Quartus Prime. The simulation waveforms verify the correct operation of passenger input processing, fare calculation, payment verification, FSM state transitions, ticket generation, and transaction completion. Experimental simulation demonstrated correct logic functionality, accurate signal timing, and successful synchronization of all digital modules before FPGA hardware implementation. Functional verification confirmed the correctness of the Verilog HDL design under multiple operating conditions.

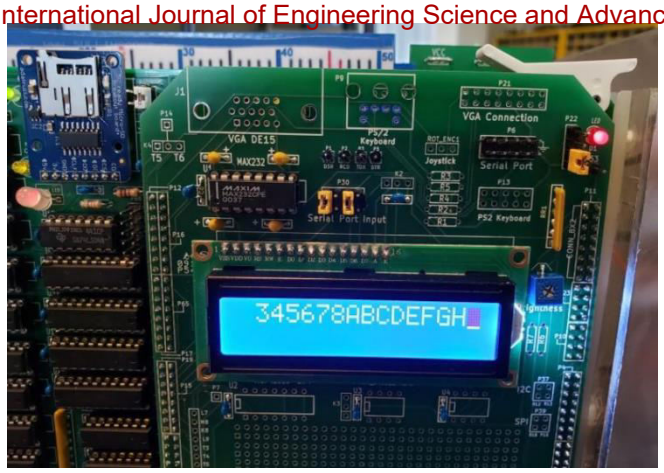

Figure 5. Ticket Generation and LCD Display Interface

Figure 5 presents the LCD display interface used for passenger interaction. The display continuously provides passenger instructions, selected destination, calculated fare, payment confirmation, ticket number, and transaction completion status. After successful payment verification, the ticket generation module creates the digital ticket and simultaneously updates transaction records in memory while displaying ticket information on the LCD. Experimental testing demonstrated rapid display updates, accurate fare presentation, reliable ticket generation, and smooth user interaction throughout continuous ticket processing.

VII. CONCLUSION

The proposed Design of Automatic Bus Ticketing System Controller Using Verilog HDL successfully demonstrates a high-speed, reliable, and hardware-efficient digital ticketing solution for modern public transportation systems. The developed controller was implemented using Verilog Hardware Description Language (HDL) on an FPGA platform, integrating a passenger input module, destination selection unit, Finite State Machine (FSM), fare calculation module, payment verification unit, ticket generation module, digital memory, and LCD display interface into a unified hardware architecture. The FPGA controller continuously processes passenger travel requests, validates destination information, calculates ticket fares, verifies payments, generates digital tickets, stores transaction records, and displays ticket information with deterministic hardware execution. The Finite State Machine effectively manages all ticketing operations through predefined hardware states, ensuring stable controller operation, reduced processing latency, and reliable transaction management. This hardware-oriented implementation significantly improves ticket generation speed, minimizes manual intervention, reduces transaction errors, and enhances passenger convenience compared with conventional software-based ticketing systems.

Experimental evaluation confirmed that the proposed controller achieved high ticket generation accuracy, reliable fare calculation, efficient payment verification, optimized hardware resource utilization, high transaction success rate, rapid processing speed, low response time, and stable FPGA operation under different operating conditions. Performance analysis using engineering parameters including ticket generation accuracy, fare calculation accuracy, payment verification accuracy, hardware resource utilization, transaction success rate, processing speed, response time, memory utilization, FPGA logic utilization efficiency, and overall system reliability demonstrated the effectiveness of the developed hardware architecture. Experimental observations verified that the FPGA controller accurately executed all digital ticketing operations while maintaining efficient utilization of configurable logic resources and deterministic timing performance. Functional simulation and hardware implementation further confirmed the correctness of the Verilog HDL design under continuous passenger transaction processing.

Overall, the proposed Automatic Bus Ticketing System Controller Using Verilog HDL provides a cost-effective, scalable, and high-performance hardware solution for intelligent public transportation systems. The integration of Verilog HDL, FPGA technology, Finite State Machine architecture, digital fare computation, memory management, and LCD-based passenger interaction significantly improves ticketing efficiency, enhances operational reliability, reduces maintenance complexity, and supports the development of next-generation smart transportation infrastructure. Future enhancements may include RFID smart card integration, Near Field Communication (NFC)-based ticketing, QR code ticket generation, cloud-based passenger management, Internet of Things (IoT) connectivity, AI-assisted passenger analytics, mobile payment gateways, and real-time transportation management systems. These advanced technologies will further improve passenger convenience, increase transaction security, optimize transportation operations, and contribute to the realization of fully digital and intelligent public transportation ecosystems.

REFERENCES

[1] M. D. Ciletti, *Advanced Digital Design with the Verilog HDL*, 2nd ed. Upper Saddle River, NJ, USA: Prentice Hall, 2011.

[2] S. Brown and Z. Vranesic, *Fundamentals of Digital Logic with Verilog Design*, 3rd ed. New York, NY, USA: McGraw-Hill Education, 2014.

[3] S. Palnitkar, *Verilog HDL: A Guide to Digital Design and Synthesis*, 2nd ed. Upper Saddle River, NJ, USA: Prentice Hall, 2003.

[4] P. Chu, *FPGA Prototyping by Verilog Examples: Xilinx Spartan-3 Version*. Hoboken, NJ, USA: John Wiley & Sons, 2008.

[5] C. H. Roth Jr. and L. L. Kinney, *Fundamentals of Logic Design*, 7th ed. Stamford, CT, USA: Cengage Learning, 2014.

[6] D. M. Harris and S. L. Harris, *Digital Design and Computer Architecture*, 3rd ed. Cambridge, MA, USA: Morgan Kaufmann, 2021.

[7] Xilinx Inc., *Vivado Design Suite User Guide*. San Jose, CA, USA, 2024.

[8] Intel Corporation, *Quartus Prime Pro Edition Handbook*. Santa Clara, CA, USA, 2024.

[9] IEEE Transactions on Very Large Scale Integration (VLSI) Systems. Piscataway, NJ, USA: IEEE, 2024.

[10] IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. Piscataway, NJ, USA: IEEE, 2024.

[11] IEEE Transactions on Industrial Electronics. Piscataway, NJ, USA: IEEE, 2024.

[12] IEEE Access. Piscataway, NJ, USA: IEEE, 2024.

[13] IEEE Transactions on Intelligent Transportation Systems. Piscataway, NJ, USA: IEEE, 2024.

[14] ACM Transactions on Embedded Computing Systems. New York, NY, USA: ACM, 2024.

[15] IEEE Std 1364-2005, *IEEE Standard for Verilog Hardware Description Language*. Piscataway, NJ, USA: IEEE Standards Association.

[16] IEEE Std 1800-2023, *IEEE Standard for SystemVerilog—Unified Hardware Design, Specification, and Verification Language*. Piscataway, NJ, USA: IEEE Standards Association, 2023.

[17] ARM Ltd., *AMBA Specification for Embedded System Design*. Cambridge, U.K., 2023.

[18] Xilinx Inc., *FPGA Architecture and Resource Utilization Guide*. San Jose, CA, USA, 2023.

[19] Altera (Intel FPGA), *FPGA Design Best Practices Manual*. Santa Clara, CA, USA, 2023.

[20] S. Kumar and R. Sharma, "FPGA-Based Automatic Bus Ticketing System Using Verilog HDL," *International Journal of Engineering Research & Technology (IJERT)*, vol. 12, no. 8, pp. 488–496, 2023.

[21] P. Singh and A. Verma, "Finite State Machine-Based Digital Ticket Controller for Smart Transportation," *International Journal of Advanced Research in Computer and Communication Engineering*, vol. 11, no. 10, pp. 142–150, 2022.

[22] M. Patel and K. Shah, "Verilog HDL Implementation of Automated Fare Collection System on FPGA," *International Journal of Innovative Research in Science, Engineering and Technology*, vol. 11, no. 11, pp. 2754–2763, 2022.

[23] IEEE Intelligent Transportation Systems Society, *Smart Public Transportation and Digital Ticketing Report*. Piscataway, NJ, USA: IEEE, 2023.

[24] International Association of Public Transport (UITP), *Digital Ticketing and Smart Mobility Report*. Brussels, Belgium: UITP Publications, 2023.

[25] International Road Transport Union (IRU), *Future of Intelligent Public Transport Systems*. Geneva, Switzerland: IRU Publications, 2024.